STANDARD CELL LIBRARY DATABOOK

version 1.0

This book documents BIT's standard cell library. The library consists of three sub-libraries, known as Control, Datapath, and I/O.

The Control library contains the most cells. It includes all cells used for random logic on the chip. Control cells are usually automatically placed and routed, and are laid out with fixed-height and variable width.

The Datapath library has more complex cells used in a datapath of a circuit, such as adders, shifters, aligners, and some miscellaneous logic cells. Since these cells are used as building blocks for a fixed-width datapath, they are laid out with fixed width and variable height. The data generally flows vertically from one row of cells to the next.

The I/O library includes all cells that interface between the internal signal levels of the chip and the outside world via the package pins. This library also contains certain cells that need special care and feeding, such as clock drivers and bias generators.

Setup times for latches and flip-flops will be in their own section towards the back of the book. For their first appearance in the databook, setup times will be estimated as the differential delay through the latch (the delay through the master latch for flip-flips).

The last section of the databook is reserved for BIT-proprietary cells and information. BIT engineers use some unique techniques in the design of shifters, adders, and other certain cells that have patents pending. For this reason, they are left out of the normal released version of the databook. As the customer begins designing with BIT's library, they may be given the datasheets for this section, depending on the need for the cells and on the customer's relationship with BIT.

Tom Arneberg
July 21, 1989

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USING THE DATASHEETS

This section of the Standard Cell Library Manual explains how to use the datasheets—specifically, how to calculate the delay of a certain path through a cell with a given capacitive load.

Any such delay consists of two components: the *intrinsic* delay for that path through the cell, and the extra delay due to capacitive load (ΔTpd). All delays in this manual are approximated with two straight lines (the last page of this section explains the reasoning behind this approach).

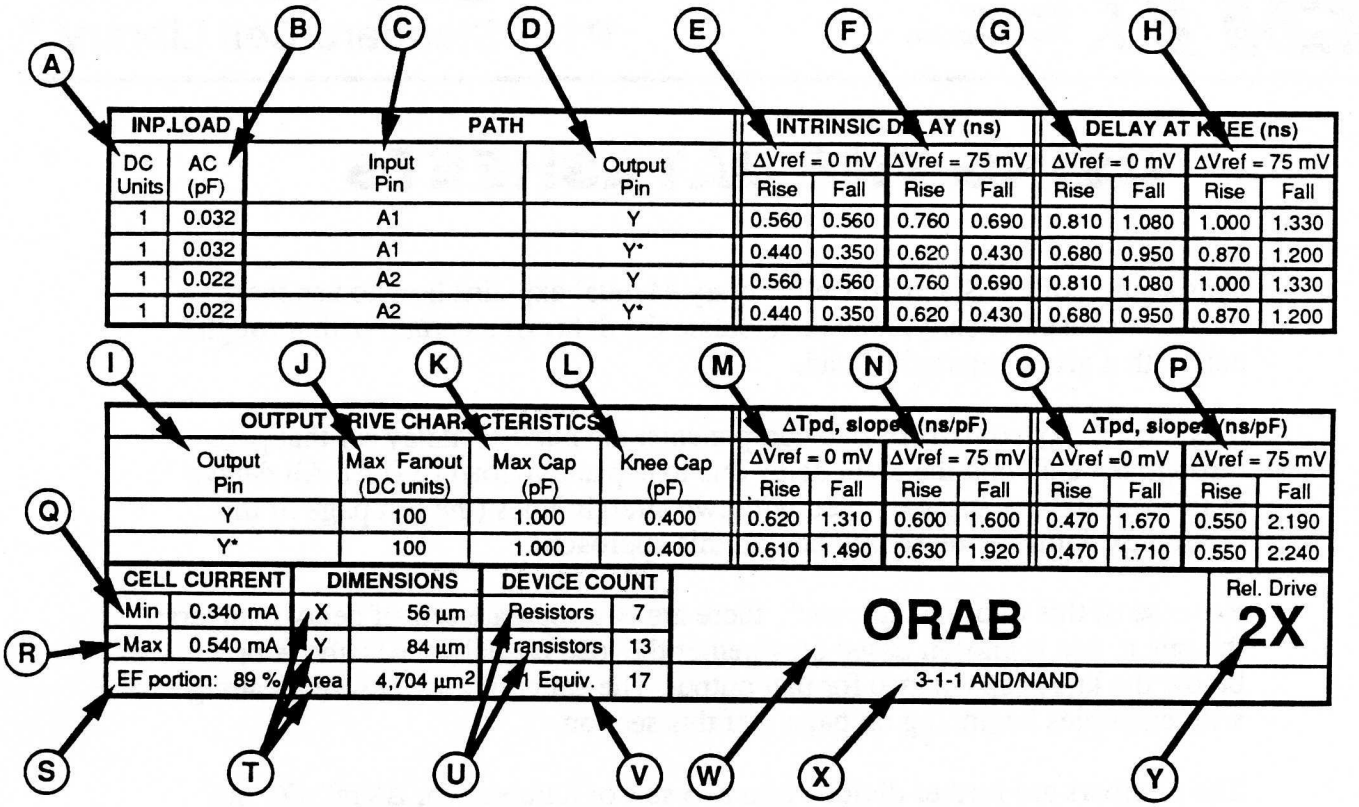
Because of this two-line approach, there are two separate sets of delay numbers; the one to use is chosen based on whether the load capacitance is above or below the knee capacitance for that output. The equations are described along with examples beginning on page 3 of this section.

The numbers are further divided into two sets of numbers for ΔVref =75 mV and ΔVref = 0 mV. These represent a combination of the IR drop of the power supply bus and the voltage reference bus, and is explained on page 5 of this section.

SPICE Parameters Used for P111 Cell Data Sheets:

Parameter	Value
Transistor Models	ts111r08.slo (worst-case process)
Resistor Values	max @ 127°C (15–25% higher than nom @ 127°C)
Junction Temperature	127 °C
Supply Voltage (VEE)	–4.65 V
Signal Swings	525 mV

DATA SHEET DESCRIPTION



INP.LOAD		PATH		INTRINSIC DELAY (ns)				DELAY AT KNEE (ns)			
DC Units	AC (pF)	Input Pin	Output Pin	ΔVref = 0 mV		ΔVref = 75 mV		ΔVref = 0 mV		ΔVref = 75 mV	
				Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
1	0.032	A1	Y	0.560	0.560	0.760	0.690	0.810	1.080	1.000	1.330
1	0.032	A1	Y*	0.440	0.350	0.620	0.430	0.680	0.950	0.870	1.200
1	0.022	A2	Y	0.560	0.560	0.760	0.690	0.810	1.080	1.000	1.330
1	0.022	A2	Y*	0.440	0.350	0.620	0.430	0.680	0.950	0.870	1.200

OUTPUT DRIVE CHARACTERISTICS				ΔTpd, slope 1 (ns/pF)				ΔTpd, slope 2 (ns/pF)			
Output Pin	Max Fanout (DC units)	Max Cap (pF)	Knee Cap (pF)	ΔVref = 0 mV		ΔVref = 75 mV		ΔVref =0 mV		ΔVref = 75 mV	
				Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
Y	100	1.000	0.400	0.620	1.310	0.600	1.600	0.470	1.670	0.550	2.190
Y*	100	1.000	0.400	0.610	1.490	0.630	1.920	0.470	1.710	0.550	2.240

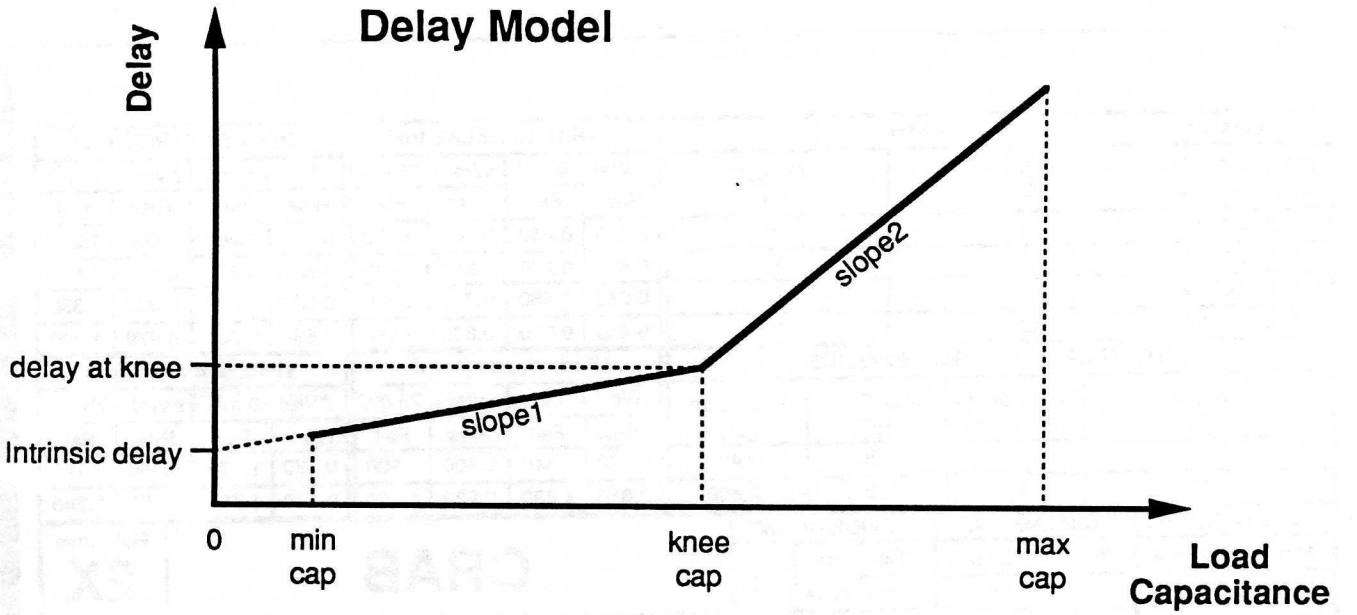
CELL CURRENT		DIMENSIONS		DEVICE COUNT			Rel. Drive
Min	0.340 mA	X	56 µm	Resistors	7	ORAB	2X
Max	0.540 mA	Y	84 µm	Transistors	13		
EF portion: 89 %		Area	4,704 µm²	T1 Equiv.	17	3-1-1 AND/NAND	

A.....Number of DC Unit Loads seen at the input
B.....Input pin capacitance (metal capacitance + transistor base capacitance)
C.....Input pin for path delay
D.....Output pin for path delay
E.....Rise & Fall delay for ΔVref = 0 mV and output load = 0 pF
F.....Rise & Fall delay for ΔVref = 75 mV and output load = 0 pF
G.....Rise & Fall delay for ΔVref = 0 mV and output load = knee capacitance
H.....Rise & Fall delay for ΔVref = 75 mV and output load = knee capacitance

I..... Output pin name
J.....Maximum DC unit load fanout of output pin
K.....Maximum capacitive drive of output pin
L.....Knee capacitance where the output slope changes
M.....Slope 1 (for load cap < knee cap), in ns/pF, of rise and fall delays for ΔVref = 0 mV
N.....Slope 1 (for load cap < knee cap), in ns/pF, of rise and fall delays for ΔVref = 75 mV
O.....Slope 2 (for load cap > knee cap), in ns/pF, of rise and fall delays for ΔVref = 0 mV
P.....Slope 2 (for load cap > knee cap), in ns/pF, of rise and fall delays for ΔVref = 75 mV
Q.....Minimum current of cell (occurs at 27 °C)
R.....Maximum current of cell (occurs at 127 °C)
S.....Portion of cell current due to emitter-followers (both input and output EFs)
T.....Physical dimensions of the cell layout (in µm)
U.....Number of resistors and transistors in the cell
V.....Number of equivalent T1's in the cell
W.....Cell name
X.....Description of cell
Y.....Output drive relative to minimum drive ("??" = mixed output drives; "W" = wired-OR output)

NOTE: ALL DELAYS IN THIS BOOK ARE FOR WORST-CASE SILICON.

The delay through a cell for any capacitive load can be calculated using the numbers on that cell's datasheet. The datasheet numbers give the intrinsic delay, the two different slopes of additional delay per picoFarad of load capacitance, and the knee capacitance where that slope changes. Using these numbers will result in the delay vs. capacitance curve below. For the entire range between minimum and maximum capacitance, this delay curve will be equal to or greater than the SPICE-simulated delay at that capacitance, and is within 3–5% for that range.



Drive	Suffix	min cap	knee cap	max cap
1X	_L	50 fF	200 fF	500 fF
2X	(null)	50 fF	400 fF	1000 fF
4X	_H	50 fF	800 fF	2000 fF
8X	_S	50 fF	1600 fF	4000 fF
16X	_U	50 fF	3200 fF	8000 fF

Values for release 1.0 of the datasheets

The minimum capacitance is the lowest capacitance found on a net in a typical design (including parasitic transistor capacitance). For a load capacitance under the minimum, the two-line approximation will *under* estimate the delay; whereas for any cap value between min and max, the two-line approximation will be conservative.

The knee cap is defined as the capacitance at the maximum error of the one-line approximation (see the *"Spice Parameters"* section of this manual).

The maximum cap is the value beyond which the signal will slow down to such a rate that noise problems can be an issue.

Delay Equations:

for Cload ≤ knee cap:

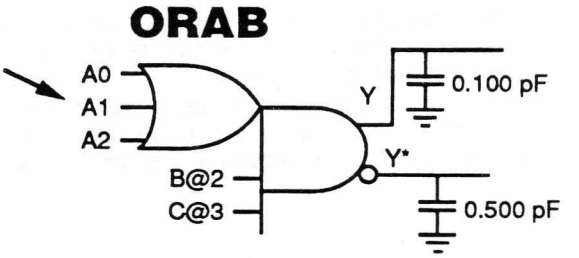
$$\text{delay(path)} = \text{intrinsic delay} + (\text{Cload}) \cdot (\text{Tpd slope1}) \qquad \text{Eq-1}$$

for Cload ≥ knee cap:

$$\text{delay(path)} = \text{delay at knee} + (\text{Cload} - \text{knee Cap}) \cdot (\text{Tpd slope2}) \qquad \text{Eq-2}$$

Example

Suppose we're interested in the delay through the cell ORAB from the input pin A1. We'd like to know the delay to both output pins; Y is loaded with 0.100 pF and Y* is loaded with 0.500 pF. Here is the delay section from that datasheet:



INP.LOAD		PATH		INTRINSIC DELAY (ns)				DELAY AT KNEE (ns)			
DC Units	AC (pF)	Input Pin	Output Pin	ΔVref = 0 mV		ΔVref = 75 mV		ΔVref = 0 mV		ΔVref = 75 mV	
				Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
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OUTPUT DRIVE CHARACTERISTICS			ΔTpd, slope1 (ns/pF)				ΔTpd, slope2 (ns/pF)			
Output Pin	Max Fanout (DC units)	Max Cap (pF)	Knee Cap (pF)	ΔVref = 0 mV		ΔVref = 75 mV		ΔVref =0 mV		ΔVref = 75 mV	
				Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
Y	100	1.000	0.400	0.620	1.310	0.600	1.600	0.470	1.670	0.550	2.190
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CELL CURRENT		DIMENSIONS		DEVICE COUNT			
Min	0.340 mA	X	56 μm	Resistors	7	ORAB	Rel. Drive 2X
Max	0.540 mA	Y	84 μm	Transistors	13		
EF portion: 89 %		Area	4,704 μm²	T1 Equiv.	17	3-1-1 AND/NAND	

We don't know how close the ORAB will be to the cell that it drives, so we'll use the worst-case ΔVref of 75 mV.

ORAB: A1 to Y; CLD = 0.100 pF; ΔVref = 75 mV

Our load capacitance is less than the knee capacitance for that output, so we use Eq.-1:

	path delay		intrinsic delay		load cap	ΔTpd slope1		
delay(A1_Y,rise)	=	.760 ns	+	(.100 pF) • (0.600 ns/pF)	=	.760 + .060	=	0.820 ns
delay(A1_Y,fall)	=	.690 ns	+	(.100 pF) • (1.600 ns/pF)	=	.690 + .160	=	0.850 ns

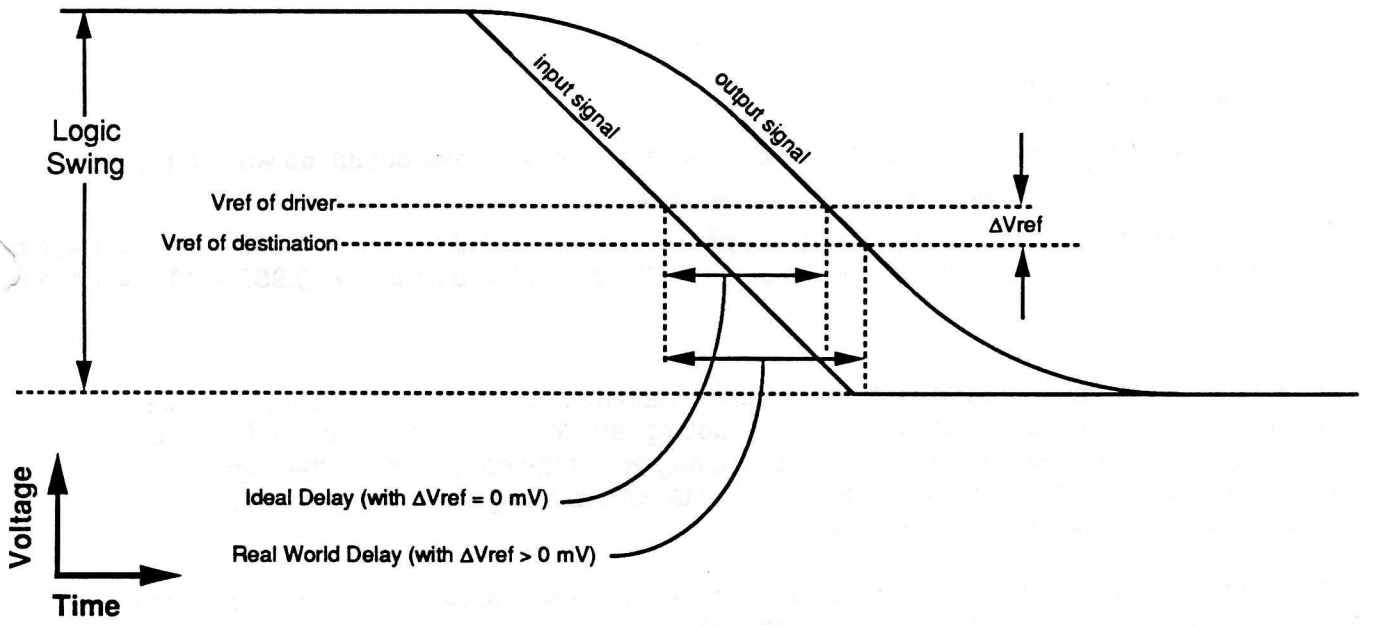
ORAB: A1 to Y*; CLD = 0.500 pF; ΔVref = 75 mV

Our load capacitance is greater than the knee capacitance for that output, so we use Eq.-2:

	path delay		delay at knee		load cap – knee cap	ΔTpd slope2		
delay(A1_Y*,rise)	=	0.870 ns	+	(.500 pF – .400 pF) • (0.550 ns/pF)	=	0.870 + .055	=	0.925 ns
delay(A1_Y*,fall)	=	1.200 ns	+	(.500 pF – .400 pF) • (2.240 ns/pF)	=	1.200 + .224	=	1.424 ns

ΔVref

In ECL, there is one threshold for both high and low transitions. The switching range of input voltage compared to the threshold voltage (called VB1, VB2, or VB3, depending on which level the signal is on) is very small compared to the full logic swing, due to the amplification characteristics of the emitter-coupled pair which make up the basis of an ECL cell. For this reason, the placement of that VB is critical to the delay of the gate. The circuit that generates VB will automatically track it in the center of the logic swing over temperature and process variations, but the Great Unknown in the equation is the IR drop of the power supply bus and the VB line, either of which can alter the relationship between the incoming logic swing and the reference to which it's compared.



The Real World delay above is longer than the ideal delay because the output signal going into the next gate takes longer to cross the next gate's threshhold, since that threshhold is lower than the center of the output signal swing.

Note that for the above set of conditions (i.e. Vref of destination gate lower than the center of the output signal), the Real World delay for a *rising* output signal would actually be *less* than the "ideal delay" by the same margin as the falling signal is greater than the ideal. The opposite is true for the case where the destination gate has a Vref higher than the center of the output signal feeding it: the rising delay would be slower, and the falling delay would be faster. In all the datasheets in this manual, the worst case is assumed for rising and for falling in the ΔVref=75mV sections.

If you have some knowledge of the proximity of the cell being driven, then the delays in the ΔVref=0 columns can enter the equation. The ΔVref is dependent on a complex set of parameters including the distance to the next cell, the current drawn in that power supply row, the current drawn in that voltage reference row, etc. Only a detailed power bus drop analysis can give an accurate answer, but you can make some reasonable assumptions if the cells are on a critical path and are placed next to each other in the same row. To get the delays under these conditions, calculate the delay at ΔVref=75 and the delay at ΔVref=0, and interpolate between the two final calculations to get the correct delay. The ΔVref=0 numbers also are useful by themselves to estimate setup times for latches, since the IR drop is zero within the same cell.

Example

Suppose we can be guaranteed due to expert cell placement that the cell we're driving will be within a certain number of microns in the same row, and so the IR drop of the supply and reference lines will be some maximum below the worst-case 75 mV. We'll use ΔVref max = 25 mV for this example, which is a realistic number for adjacent cells.

ORAB: A1 to Y*; CLD = 0.500 pF

Our load capacitance is greater than the knee capacitance for that output, so we use Eq.-2:

ΔVref	path delay		delay at knee		load cap – knee cap		ΔTpd slope2		
75 mV	delay(A1_Y*,fall)	=	1.200 ns	+	(.500 pF – .400 pF)	•	(2.240 ns/pF)	= 1.200 + .224	= 1.424 n
0 mV	delay(A1_Y*,fall)	=	0.950 ns	+	(.500 pF – .400 pF)	•	(1.710 ns/pF)	= 0.950 + .171	= 1.121 n

Notice the large difference in delays for the exact same path through the same cell under the exact same conditions of silicon, temperature, capacitive loading, etc. In fact, the output of the ORAB is doing exactly the same thing in both cases; it's the *perception* of the cell accepting that signal that changes the apparent delay. This large difference points out that using the worst-case 75mV Vref numbers for every gate can be overly conservative.

Now, getting the delay for our more reasonable close cell whose reference and swing are not more than 25 mV different than the ORAB is just a matter of simple linear interpolation:

$$\text{delay(IR mV)} = \text{delay(0 mV)} + (\text{IR}/75) \cdot [\text{delay(75 mV)} - \text{delay(0 mV)}], \text{ where IR} = \Delta\text{Vref}$$

$$\text{delay(25 mV)} = \text{delay(0 mV)} + (25/75) \cdot [\text{delay(75 mV)} - \text{delay(0 mV)}]$$

$$= 1.247 \text{ ns} + (1/3) \cdot [1.549 - 1.247] = 1.247 + .101 = 1.348 \text{ ns}$$

BALLPARK CAPACITANCE NUMBERS FOR PROCESS 111:

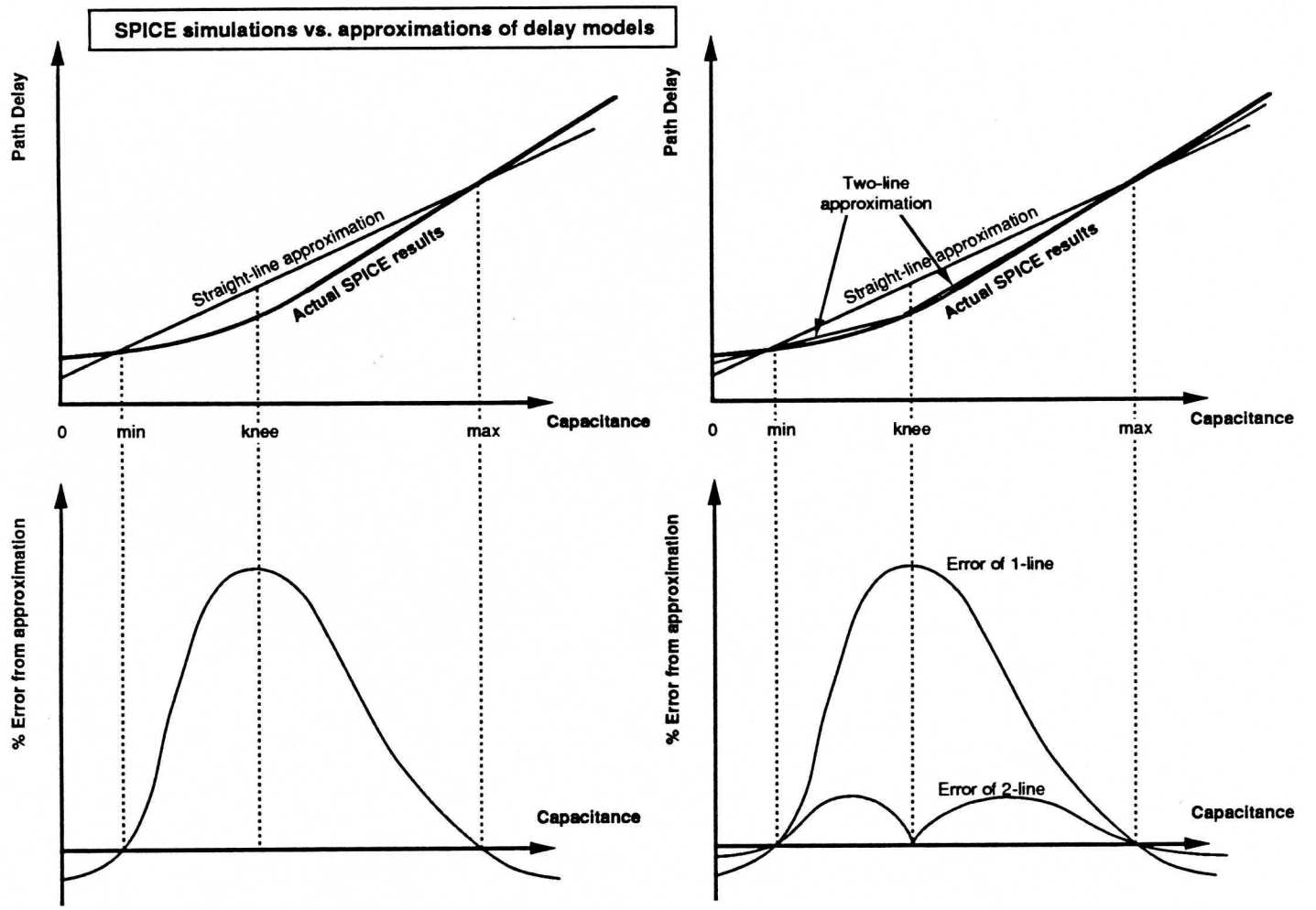
Routing Capacitance
metal 1...0.34 fF/μm length
metal 2...0.24 fF/μm length
metal 3...0.20 fF/μm length

Cell Input Capacitance
20 fF per T1 input transistor base
plus 2–40 fF for internal cell metal
(see AC Unit Load in cell data sheets)

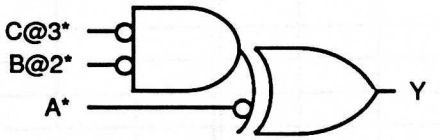
SPICE Approach to Cell Circuit Simulation

BIT uses a two-line approximation for the delay due to capacitive loading. In several simulation experiments, the error between a one-line approximation and the real SPICE results often were in the range of 15%. Second and third-order polynomial approximations were even worse, since the ideal delay vs capacitance curve goes to a straight line as capacitance gets higher. But the two-line approximation is well within 5% (usually 2–3%) of the actual SPICE results for any capacitance within the range specified for that output.

The "knee" capacitance is defined as the capacitance value at the maximum of the %error curve of the one-line approximation, so that the error of the two-line approximation is minimized.



The entire library of cells is actually simulated with SPICE twice: once to get the delay of all paths through the cell at one capacitance (the knee), and another time to toggle each output at three capacitances (the min, the knee, and the max) to get the ouput loading slope in ns/pF. The reason we went through the extra effort to calculate every output slope separately is that we have seen up to a 40% difference in output loading slopes for identical output sizes, depending on the internal loading of the base of the output transistor. But since the slope of a given output is independent of the path through the cell, we used the simplest combination of inputs that would toggle the output for those SPICE runs.



$Y = A^* \oplus (B@2^* + C@3^*)$

Cell Base: **DPORXORA**
Library: DATAPATH
Description: 2-1 AND-XOR

SPICE: Worst-case process transistor models (ts111r08.slo), maximum resistors (+ 3 sigma), at 127° C

INP.LOAD		PATH		INTRINSIC DELAY (ns)				DELAY AT KNEE (ns)			
DC Units	AC (pF)	Input Pin	Output Pin	ΔVref = 0 mV		ΔVref = 75 mV		ΔVref = 0 mV		ΔVref = 75 mV	
				Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
1	0.057	A*	Y	0.410	0.340	0.570	0.410	0.580	0.970	0.750	1.240
1	0.029	B@2*	Y	0.590	0.660	0.730	0.730	0.760	1.290	0.910	1.560
1	0.034	C@3*	Y	0.550	0.610	0.700	0.680	0.720	1.240	0.880	1.510

OUTPUT DRIVE CHARACTERISTICS				ΔTpd, slope1 (ns/pF)				ΔTpd, slope2 (ns/pF)			
Output Pin	Max Fanout (DC units)	Max Cap (pF)	Knee Cap (pF)	ΔVref = 0 mV		ΔVref = 75 mV		ΔVref =0 mV		ΔVref = 75 mV	
				Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
Y	50	0.500	0.200	0.860	3.130	0.900	4.150	0.690	3.610	0.770	4.710

CELL CURRENT		DIMENSIONS		DEVICE COUNT	
Min	0.200 mA	X	56 µm	Resistors	5
Max	0.340 mA	Y	76 µm	Transistors	12
EF portion: 66 %		Area	4,256 µm2	T1 Equiv.	12

DPORXORA_L

2-1 AND-XOR

Rel. Drive **1X**